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INTEGRATED FLOATING POWER TRANSFER DEVICE WITH ELECTROMAGNETIC EMISSION CONTROL CIRCUIT AND METHOD

This application claims the benefit of U.S. Provisional No. 60/427,413, filed November 18, 2002. This provisional application is hereby incorporated by reference herein in its entirety.

The present invention relates in general to power transfer devices, and more particularly, to a switch control circuit and method for constraining electromagnetic emissions from an integrated floating power transfer device.

Many system designs include power conversion circuitry to develop a required operating voltage. One such power conversion circuit is known as a charge pump. A charge pump is a device for creating increases in supply voltage or for inverting a supply voltage to generate a split supply. Many of these devices are related to applications using non-volatile memory circuits, which require a high voltage for programming. In a conventional charge pump power conversion circuit, the load device connects so that one terminal thereof is common to one of the supply terminals, typically the ground reference. U.S. Letters Patent No. 4,807,104 discloses a power conversion circuit which is both a voltage multiplying and inverting charge pump. However, the output of the power conversion circuit remains referenced to the ground node.

In certain system implementations, it may be advantageous to power the system using a floating power transfer device. By floating the power transfer device, if a terminal in the system were to short, then the system may still be able to continue to operate. For example, in an automobile bus network, the signaling portion of the system on the bus could be floating relative to any other reference, such as ground or battery positive. This would provide enhanced fault tolerance by allowing communications to still occur notwithstanding a short at a terminal thereof.

The shortcomings of the prior art are overcome and additional advantages are provided by the provision of a floating power transfer device which includes a floating bus, and a power and data system for driving the floating bus. The power and data system include a charge pump circuit. Electromagnetic emission control is provided by at least one switch control circuit coupled between the floating bus and the power and data system for facilitating charging of the floating bus and controlling electromagnetic emissions from the floating bus by constraining a slew rate on the floating bus.

In another aspect, a circuit is provided which includes a first switch control circuit for electrically coupling to a high side bus node of a floating bus, and a second switch control circuit for electrically coupling to a low side bus node of the floating bus, wherein the first switch control circuit and the second switch control circuit comprise
5 complementary control circuits for controlling charging of the floating bus by a power and data system. A reference circuit is also provided for generating a first reference signal for the first switch control circuit and a second reference signal for the second switch control circuit. The first reference signal and the second reference signal are employed by the first switch control circuit and the second switch control circuit, respectively, for controlling
10 electromagnetic emissions from the floating bus by constraining a slew rate on the floating bus.

In a further aspect, a method for constraining electromagnetic emissions from an integrated floating power transfer device is provided. This method includes: tailoring a transfer characteristic of a first switch control circuit to be electrically coupled to a high side
15 bus node of a floating bus, and tailoring a transfer characteristic of a second switch control circuit to be electrically coupled to a low side bus node of the floating bus, wherein the first switch control circuit and the second switch control circuit comprise complementary control circuits for controlling charging of the floating bus by a power and data system; and generating, when in use, a first reference signal for the first switch control circuit and a
20 second reference signal for the second switch control circuit, wherein the first reference signal and the second reference signal are employed by the first switch control circuit and the second switch control circuit, respectively, for controlling electromagnetic emissions from the floating bus by constraining a slew rate on the floating bus.

Additional features and advantages are realized through the techniques of the
25 present invention. Other embodiments and aspects of the invention are described in detail herein and are considered a part of the claimed invention.

The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the invention are apparent from the following
30 detailed description taken in conjunction with the accompanying drawings in which:

FIG. 1 is a schematic of one embodiment of a conventional voltage-doubling charge pump circuit;

FIG. 2 is a schematic of one embodiment of a floating power transfer device which enables the dual function of power and data transfer;

FIG. 3 is a schematic of one embodiment of an integrated circuit implementation of a floating power transfer device;

5 FIG. 4 is a schematic of one embodiment of an integrated floating power transfer device having switch control circuits for limiting electromagnetic emissions, in accordance with an aspect of the present invention;

10 FIG. 5 is a graph of a transfer characteristic for a switch control circuit for the integrated floating power transfer device of FIG. 4, in accordance with an aspect of the present invention;

FIG. 6 is a schematic of one embodiment of a switch control circuit for the integrated floating power transfer device of FIG. 4, in accordance with an aspect of the present invention;

15 FIG. 7 is a schematic of one embodiment of a N type transistor level implementation of the switch control circuit of FIG. 6, in accordance with an aspect of the present invention;

FIG. 8 is a schematic of an enhanced N type transistor level implementation of the switch control circuit of FIG. 6, in accordance with an aspect of the present invention;

20 FIG. 9 is a schematic of another enhanced N type transistor level implementation of the switch control circuit of FIG. 6, in accordance with an aspect of the present invention; and

FIG. 10 is a schematic of one embodiment of a P type transistor level implementation of a switch control circuit such as shown in FIG. 7, in accordance with an aspect of the present invention.

25 Reference is now made to the drawings, wherein the same reference numbers used throughout different figures designate the same or similar components. One embodiment of a power transfer device for powering a load 105 is shown in FIG. 1. This charge transfer device delivers charge onto a capacitor CS 103 through switches SW4, SW3 101, 110 under control of a signal generator 109. Charge is provided by a power supply voltage (V_{DC}) 107, one side of which is referenced to ground 108. A capacitor CH 104 provides the
30 modified power supply for load 105. In this voltage doubling example, capacitor 104 is charged with double the voltage of capacitor CS when switches SW1, SW2 102, 111 are closed by signal generator 106.

The power transfer device of FIG. 1 is referred to as a ground referenced charge transfer device since the device supplies power to the load via a ground referenced capacitance. Circuits such as depicted in FIG. 1 are often used in applications such as E²ROM programming or extending the operating range of diverse analog circuits. As explained further below, the present invention does not necessarily seek to increase or invert an output voltage, but rather employs a similar switching scheme to precharge a floating bus with a voltage that is close to the original source-voltage. A circuit implemented in accordance with an aspect to the present invention is designed to allow power to be drawn continuously from the floating circuit, while a signaling scheme may partially or completely discharge the floating bus. The combined power and data feature of this apparatus has been previously described in commonly assigned European patent document EP 1 065 600 A2, the entirety of which is hereby incorporated herein by reference.

One embodiment of a floating power transfer device that enables the dual function of power and data transfer is shown in FIG. 2. A floating bus is a bus that is electrically isolated from the ground reference 108 of the source voltage V_{DC} 107. In the circuit depicted in FIG. 2, the output VB+ 216 provides a continuous power source relative to the floating bus, which is defined as the two nodes BUS+ 214 and BUS- 215. During the "data" phase when signal generator V_{SW1} 109 is at a logical 1, the source switches SW3, SW4 110, 101 are "on" and the source voltage is driven onto the shuttle capacitor CS 103. The output switches SW1, SW2 102, 111 are "off" and the floating bus BUS+ 214 and BUS- 215 is available for signaling purposes. Power is available from the floating bus due to the energy retained by the hold capacitor CH 204. A diode 212 prevents the bus signal voltages from discharging the hold capacitor 204. A "power" phase, when signal generator V_{SW2} 106 is at a logical 1, completes the two-phase cycle by turning on the bus switches 102, 111, while V_{SW1} 109 returns a logic zero, turning off the source switches 101, 110. During this period, charge is delivered from the shuttle capacitor 103 to the floating bus 214, 215, and consequently to the hold capacitor 204. The voltage on the floating bus is restored to a value close to the source voltage. Depleted charge from the hold capacitor 204 is restored, while maintaining the continuous source of power from output VB+ 216, as required.

An integrated circuit (IC) implementation of a floating power transfer device with a combined power and data feature is shown in FIG. 3. In this implementation, switches 101, 110 and 102, 111 are replaced by DMOS transistors 301, 310 and 302, 311, which are P

type and N type transistors. These devices require the addition of diodes 317, 318, 319, 320 to maintain the isolation of the floating bus BUS+, BUS- 214, 215 from the source voltage 107 and ground 108. This means that there are additional electrical losses in this form of the circuit and the available output voltage relative to the original source voltage is reduced.

5 The signal generators 106, 109, now require additional complementary control sources 109b, 106b to drive the P-type DMOS transistor switches 301, 302 (with the N-type DMOS transistor switches 310, 311 being driven by control sources 109, 106, respectively).

Typically, the control sources are driven by digital signals, biased at the prevailing logic-supply voltage, with the same phasing as described above in connection with the floating
10 power transfer device of FIG. 2.

Power is again available in this implementation from the floating circuit due to energy retained by the hold capacitor CH 204. Diode 212 again prevents the bus signal voltages from discharging the hold capacitor 204. Output VB+ 216 at one side of load 205 provides a continuous power source relative to the floating bus.

15 When a signal appears on the floating bus during the data phase, it may drive the bus voltage to 0 V or some other predetermined intermediate value. For the remainder of this phase, the bus is held at that value. At the commencement of the power-phase, the bus transistor switches 302, 311 turn on and the bus voltage is restored to the power level. In this system, the speed at which the bus voltage changes is dependent on the impedance of
20 the switches 302, 311 and diodes 318, 319 conducting current from the shuttle capacitor CS 103 onto the floating bus. When the rate of change is uncontrolled, as in this case, the edge of the voltage waveform can be quite sharp. This results in a signal spectrum with a high harmonic content. If the spectral content of the signal spreads into adjacent radio bands, then this is called electromagnetic emission (EME). Certain applications of a floating
25 power transfer device such as depicted in FIG. 3 may require the system to limit the EME to a minimum. In one aspect, the present invention provides a technique for reducing/constraining the EME generated by the floating supply circuit.

Disclosed herein is a technique for constraining the EME output from a floating bus driven by a combined power and data system and based on an integrated circuit (IC) charge
30 pump circuit. As noted above, the uncontrolled slope of the power-phase voltage edge can generate EME that interferes with radio reception. Replacing the bus-switch transistors 302, 311 of FIG. 3 with special switch control circuits as disclosed herein improves the EME performance of a target power transfer device. In one example, the transfer device is

assumed to have two operating modes, a high-speed mode and a low-speed mode. It is possible to achieve a better EME performance in the low-speed mode by taking advantage of the longer time interval available to deliver charge onto the bus. This means that, in certain implementations, the switch control circuits have a selectable mode of operation that is dependent on the bus speed.

The floating bus forms a balanced system where the high-side BUS+ 214 switch 302 and diode 318 are matched by a corresponding low-side BUS- 215 switch 311 and diode 319, and which includes the implicit bus capacitance CBUS 213. The current flow is out of the BUS+ and into the BUS- terminal. Two complementary circuits are used to maintain the balance of the system, while achieving the reduction in EME that is desired. The circuit shown in FIG. 4 depicts one embodiment of a floating power transfer device with EME control.

In FIG. 4, the source-side switches 301, 310 and diodes 317, 320 remain as described in FIG. 3, while the BUS-side switches are replaced by switch control circuits 402, 411 and a reference circuit 421. Switch control circuit 402, in this example, is P-type transistor based and provides a controlled current output, while switch control circuit 411, in this example, provides an N-type transistor controlled current output. The reference circuit 421 provides two stable, temperature compensated reference signals that are used in setting operation of the switch control circuits 402, 411.

The conceptual operation of the switch control circuits 402, 411 is similar for both the "Pcontrol" 402 and the "Ncontrol" 411 circuits, with the N version being described in detail herein. The "Pcontrol" circuit 402 would comprise the complement of the N circuit. The "Ncontrol" circuit has a control input Ctrl and a reference Ref as well as the switch nodes Vlo and Sw. When a logical 1 is applied to the Ctrl input, the switch control circuit 411 is turned on, and with a logical 0, it is off. When the voltage across the switch terminals Sw and Vlo is larger than a given threshold voltage (V_{swTh}), the output current is kept at a constant value, dependent on the reference value.

A graphical view of one example of the voltage-current relation (i.e., transfer characteristic) for the "on" switch is shown in FIG. 5 for a device that limits the output current to, for example, 200mA for switch voltages greater than 1V.

In the circuit of FIG. 4, the negative switch voltage is not possible because of the blocking diode D₁ 319. At switch voltages less than 1V there is insufficient voltage to maintain the limit current and output current becomes a function of the switch voltage.

When the switch voltage is 0V, the current is also 0. As noted, reference block RefGen 421 provides separate references for the two complementary switch control circuits 402, 411. In the example of FIG. 4, a current is used to provide the reference, but a voltage may also be used.

5 The HiLo input to the RefGen circuit 421 is used to select between two different reference current levels that are determined by the bus speed. During high speed operation, the current is fixed at the maximum level that develops the necessary slew rate for the bus through the switch control circuits 402, 411. With low speed operation, a period of low current is specified prior to the application of the maximum output level. This creates a
10 longer slew, and thus reduces the EME in the low speed mode.

To restate, switch control circuits 402, 411 are provided in this example to limit current to a fixed value so that with a rising voltage on the floating bus, the amount of electromagnetic emissions is controlled. The amount of EME depends upon the sharpness of the switch on and switch off characteristics of the switch control circuit. FIG. 5 depicts
15 one example of a desired transfer characteristic for the Ncontrol 411 circuit of FIG. 4. The slope shown in FIG. 5 determines the effective resistance of the switch. In the first phase, while the current and voltage are rising, EME is generated, while in the second phase the current remains substantially stable and is used to place charge onto the hold capacitor 204 and bus capacitor CBUS 213. The Vswitch in FIG. 5 represents the voltage difference
20 between Vlo and Sw in Ncontrol circuit 411. As the voltage increases, the output current also increases until the Vsw equals approximately 1 volt, at which point the current becomes a constant 200 mA.

One embodiment of the N control circuit 411 is depicted in FIG. 6. In this embodiment, the function $F(V_{ctrl}, V_{Out})$, controls the output current Iout 601 based on the
25 comparison between the reference voltage VRef resulting from the current generated by the source 609 flowing through resistance R1 604 to ground 603. Reference voltage VRef comprises one input to an error amplifier 608, which has a second input of VCmp, created by the output current flowing through resistor R0 605. The ratio between the resistor values R1 604 and R0 605 allows scaling between the output and reference currents. The control
30 operator 606 ensures that the output current remains essentially constant as the output voltage changes. As VOut approaches the same values as VCmp, the output regulation is unable to maintain the full output current and the current reduces. Switch 610 turns off the output current Iout 601 when the switch is "on", under the control of signal Vsw 611.

Resistor R2 612 allows the control VCtrl to be pulled to 0V to ensure that the output is fully disabled.

FIG. 7 depicts one transistor level implementation of an "Ncontrol" circuit such as described above in connection with FIG. 6.

With this design, the output is partitioned into two branches controlled by DMOS switches MND1 717 for BranchA and MND0 716 for BranchB. Splitting the output current into two paths allows a small series-resistance RBA 714 in BranchA to create a sense voltage to be compared to the generated reference voltage, without introducing additional resistance into the main current path, BranchB.

The input node Iref 722 supplies the reference current I_R that is folded through current mirrors J_4, J_3, J_5 721, 712, 711. The mirrors J_2, J_1, J_0 708, 706, 705 fold the reference current from the positive supply. Mirror J_0 705 doubles the output current to $2 \cdot I_R$ and provides the correct biasing current I_R for diode-connected NMOS transistor M2 720 and the remaining current (also I_R) is used to create an offset voltage across resistor RIB 718. An identical current I_R biases the two NMOS transistors M3 703 and M2 720. Device M3 703 provides the gain of the circuit. The voltage $I_o \cdot RBA$ is compared to the reference voltage obtained from $I_R \cdot RIB$, the additional resistor RIA 719 corrects for the small error introduced by the addition of the reference current I_R to the output current in BranchA. With the current I_R in each path, the values of resistors R0, RIA and RIB are identical. The final value of the output current I_{out} 701 through the blocking diode D_2 702 is obtained from the following:

$$I_o = \frac{I_R \cdot RIB}{RBA}$$

$$I_{out} = I_o \cdot (N+1)$$

The offset at the source of transistor MND1, created by the current through RBA 714, is compensated at the gate drive nodes GateBA and GateBB by the resistor R0 704. When the circuit is operating in equilibrium the current through R0 704 is the same as the current in RIB 718, and both devices have the same voltage. The feedback loop around R0 704, MND1 717, RBA 714, M2 720, RIB 718 and M3 703 ensures that the voltage across R0 704 is the same as that across RBA 714. This condition remains true while the output voltage on the drain node remains sufficient to keep both DMOS switches MND1 717 and MND0 716 in saturation. In dynamic conditions, such as the pull-down of the output on node Iout, and consequently on the drain, an amount of charge is lost to the gate of MND1 717 that creates an error in the voltage drop across R0 714. Similarly, an additional error is

introduced by the current lost in charging the gate of MND0 716 that alters the bias condition of NMOS transistor M3 703. If the gate charging current is small relative to the bias current then the accuracy of the output current $(N+1) \cdot I_o$ is sufficient for the purposes of this apparatus.

5 The switching of the output node is achieved by a control signal Vsw 710 that drives the gate switches SW_0 713 and SW_1 715. When the switches are turned on, the two gate nodes GateBA and GateBB are pulled down to ground, turning off both of the output DMOS transistors, MND1 717 and MND0 716. The current loss through the switches is limited by the current mirror J_1 706 to be I_R .

10 Errors introduced by the output Iout 701 slewing mentioned in connection with FIG. 7, can be addressed by the circuit shown in FIG. 8. Two scaled class-B amplifiers 825, 826 are used to buffer a replication of the original amplifier output-stage. This is formed by the addition NMOS transistor N_9 824, resistor ROX 823 and current mirror J_6 827. The N:1 scaling at the output devices (MND1 817, MND0 816) requires a similar
15 scaling in the gate current. This is achieved by scaling the buffers, with the buffer 825 driving GateBB being N times the strength of the buffer 826 that drives node GateBA. When the circuit turns on, the output Iout begins to fall inducing current in the gate nodes due to the parasitic gate-capacitance on the output DMOS devices. When this happens, the buffers turn on and supply the additional current into the gate nodes. As equilibrium is
20 achieved, the buffer stops supplying the additional current.

 Returning to FIG. 7, when the output is disabled, the amplifier limits, with its gain transistor M3 703 driven into an off state. The switches 713, 715 sink the bias current I_R that is also lost through the other stages. An additional variation of the circuit of FIG. 7 is depicted in FIG. 9. FIG. 9 provides an improvement in the switching time from control
25 input to control output. To reduce the power losses in the circuit, a variation in the circuit splits the bias current sources into two parts for each branch. One part remains static, while the second part is switched. A separate control signal 924, two additional switches 925 and 926, with mirror devices 927 and 923 are combined to form the enhancements to the basic switch control circuit of FIG. 7. Keeping the circuit partly biased ensures that the startup of
30 the circuit is improved. The overall current ratios are maintained so that when the circuit is on, the circuit behaves identically to that of FIG. 7.

 The enhancements of FIG. 8 and FIG. 9 may also be combined into a single switch control circuit to obtain both the described improvements. In a full circuit implementation,

the current mirrors may require cascoding to increase their output impedance. The use of cascode devices depends on the accuracy required for the output current I_{out} .

One embodiment of the complementary "Pcontrol" circuit is depicted in FIG. 10. FIG. 10 is essentially a PMOS/PDMOS version of the circuit of FIG. 7. Mirrors that were
5 connected to ground in FIG. 7 now connect to the positive supply, and vice-versa for the remaining mirrors. P-type devices replace any N-type devices, and the operation of the circuit remains the same.

Although preferred embodiments have been depicted and described in detail herein,
it will be apparent to those skilled in the relevant art that various modifications, additions,
10 substitutions and the like can be made without departing from the spirit of the invention and these are therefore considered to be within the scope of the invention as defined in the following claims.